PE 2818

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Xiaowei Deng, et al.	Docket No:	TI-31071
Serial No:	09/976,983	Conf. No:	3329
Examiner:	Trong Q. Phan	Art Unit:	2818
Filed:	10/12/2001		
For:	LOADLESS 4T SRAM CELL WITH PMOS DRIVERS		

APPEAL BRIEF UNDER 37 C.F.R. 1.192

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this Appeal Brief filed, in triplicate, under 37 CFR 1.192 is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 8-28-03.

Ann Trent
Ann Trent

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed April 15, 2003, and the Advisory Action mailed June 23, 2003.

Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

Claim 1 was rejected. Claim 1 is appealed.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

There are no amendments filed after the final rejection under 37 C.F.R. 1.192(c)(4)

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

The instant invention is a memory cell that operates over a wide range of temperatures. The memory cell has numerous advantages over memory cell structures used in the art.

The memory cell of the instant invention is formed by interconnecting PMOS drive transistors and NMOS pass transistors to wordlines, bitlines, and a supply voltage. In particular a PMOS drive transistor has one of its source/drain terminals connected to a supply voltage. The other source/drain terminal of the PMOS drive transistor is connected to a first storage node and the gate terminal of the PMOS drive transistor is connected to second storage node (page 5, lines 7-21). A NMOS pass transistor has one of its source/drain terminals connected to a bitline. The second source/drain terminal of the NMOS pass transistor is connected to the first storage node and the gate terminal of the NMOS pass transistor is connected to a wordline (page 5, lines 21-30).

An important condition of the memory cell is that for the same voltages applied across the gate and source/drain terminals of the NMOS pass transistor and the gate and source/drain terminals of the PMOS drive transistor, the current which flows through the source/drain terminal of the NMOS pass transistor must be greater than the current which flows through the source/drain terminal of the PMOS drive transistor. The condition applies to all NMOS and PMOS transistors in the memory cell. This condition can be achieved using well-known NMOS and PMOS transistor design and processing techniques (page 5, lines 32-33, page 6, lines 1-10).

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

1. Is claim 1 properly rejected under 35 U.S.C. 112, first paragraph and second paragraph?
2. Is claim 1 properly rejected under 35 U.S.C. 102(e) as being anticipated by Leung et al.?

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

There is only a single claim on appeal. Claim 1 will stand or fall based on the out come of the appeal.

Arguments

Is claim 1 properly rejected under 35 U.S.C. 112, first paragraph and second paragraph?

Appellants contend that claim 1 is not properly rejected under 35 U.S.C. 112, first paragraph.

In forming the rejection of claim 1 under 35 U.S.C. first paragraph the examiner stated in an action dated April 13, 2003 the following, "The voltage across the gate and source/drain terminals of each the NMOS pass transistors and the voltage across the gate and source/drain terminals of the PMOS pass transistors in Fig. 3 of the present invention can not be the same since they are not the same type of transistor and they are not connected in the same connection."

The language in claim 1 to which the examiner is referring is the following, "for the same voltages applied between the gate and source/drain terminals of the PMOS drive transistor and the gate and source/drain terminals of the NMOS pass transistor." The claim specifically refers to voltages applied between the gate and source/drain terminals of the PMOS drive transistor and the gate and source/drain terminals of the NMOS pass transistor. The claim refers to specific voltages applied to specific terminals of the NMOS and PMOS transistor. Clearly voltages applied to the transistors are not dependent on the

type of transistor. In addition the transistors do not have to be connected in the same connection to have specific voltages applied to the terminals as outlined in the claim.

The examiners basis for rejecting claim 1 over 35 U.S.C. 112 first paragraph is flawed and claim 1 is allowable over 35 U.S.C. 112 first paragraph.

Appellants contend that claim 1 is not properly rejected under 35 U.S.C. 112, second paragraph.

In forming the rejection of claim 1 under 35 U.S.C. second paragraph the examiner stated in an action dated April 13, 2003 the following, "No antecedent basis for "the same voltages" (line 21). Referring to page 5, lines 32-33, it is stated in the disclosure that for the same voltages applied across the gate and source/drain terminals of the NMOS and PMOS transistors the resulting current in the NMOS transistor must be greater than the current in the PMOS transistor. There is clearly antecedent basis for "the same voltages" in claim 1 and claim 1 is allowable over 35 U.S.C. 112 second paragraph.

Claim 1 stands rejected under 35 U.S.C. 102(e) as being anticipated by Leung.

In an action date 4/13/2003 the examiner states that during a read operation, the voltage applied to the word line 505 must be equal to the Vcc power supply voltage at node N1 minus the source-to-gate Vgs of the NMOS pass transistor 501 or must be less than 90% of the Vcc power supply voltage during the read operation as recited in claim 1. This statement represents a complete misunderstanding of the cited art and circuit operation in general. The voltage applied to the word line is independent of any voltage that may or may not be on N1 as well as any Vgs voltage drop. The examiner is directed to Figure 5 and the wordline 505. Any voltage can applied to word line 505. As is clear from the Figure, the applied voltage is independent of any voltage that exists in the circuit. Under the current understanding of MOS transistor circuit theory the examiners statement has little meaning. The limitation of claim 1, "during a read operation a voltage applied to the wordline is less than 90% of the supply voltage" is

neither taught nor disclosed in the cited art. As such claim 1 is allowable over the cited art.

Is claim 1 properly rejected under 35 U.S.C. 102(e) as being anticipated by Leung et al.?

Appellants contend that claim 1 is not properly rejected under 35 U.S.C. 102(e) as being anticipated by Leung et al.

In an action date 4/13/2003 the examiner states that during a read operation, the voltage applied to the word line 505 must be equal to the Vcc power supply voltage at node N1 minus the source-to-gate Vgs of the NMOS pass transistor 501 or must be less than 90% of the Vcc power supply voltage during the read operation as recited in claim 1. This statement represents a complete misunderstanding of the cited art and circuit operation in general. The voltage applied to the word line is independent of any voltage that may or may not be on N1 as well as any Vgs voltage drop. The examiner is directed to Figure 5 and the wordline 505. Any voltage can be applied to word line 505. As is clear from the Figure, the applied voltage is independent of any voltage that exists in the circuit. The limitation of claim 1, "during a read operation a voltage applied to the wordline is less than 90% of the supply voltage" is neither taught nor disclosed in the cited art. As such claim 1 is allowable over the cited art.

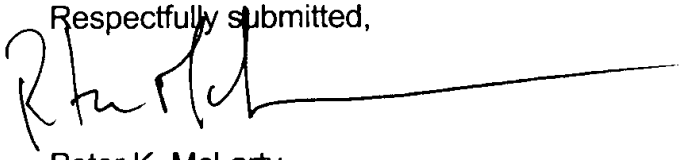
Conclusion

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claim 1 under 35 U.S.C. § 112 and 35 U.S.C. § 102 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper,

including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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APPENDIX

Claims on Appeal

1. A memory cell, comprising:

providing a PMOS drive transistor with a gate terminal, a first source/drain terminal, and a second source/drain terminal;

providing a NMOS pass transistor with a gate terminal, a first source/drain terminal and a second source/drain terminal;

connecting said first source/drain terminal of said NMOS pass transistor to a bitline;

connecting said second source/drain terminal of said NMOS pass transistor to a first storage node;

connecting said gate terminal of said NMOS pass transistor to a wordline;

connecting said first source/drain terminal of said PMOS drive transistor to a supply voltage;

connecting said second source/drain terminal of said PMOS drive transistor to said first storage node;

connecting said gate terminal of said PMOS drive transistor to a second storage node; and

wherein a current flowing through the source/drain terminals of the NMOS pass transistor is greater than a current flowing through the source/drain terminals of the PMOS drive transistor for the same voltages applied between the gate and source/drain

terminals of the PMOS drive transistor and the gate and source/drain terminals of the NMOS pass transistor and during a read operation a voltage applied to the wordline is less than 90% of the supply voltage.